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SRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS

Abstract of the Disclosure

Structures and methods are provided for SRAM cells having a novel, non-volatile floating gate transistor, e.g. a non-volatile memory component, within the cell which can be programmed to provide the SRAM cell with a definitive asymmetry so that the cell always starts in a particular state. The SRAM cells include a pair of cross coupled transistors. At least one of the cross coupled transistors includes a first source/drain region and a second source/drain region separated by a channel region in a substrate. A floating gate opposes the channel region and separated therefrom by a gate oxide. A control gate opposes the floating gate. The control gate is separated from the floating gate by a low tunnel barrier intergate insulator.